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Greenbank Electronics

Use of Carter Model 756 Keyboard with Kemitron DCR-6 Board And Further Notes on the DCR-6 Board Itself

Introduction: Although we have not used the Carter Model 756 Keyboard ourself, we have looked through their published data and have prepared the following notes which we hope will assist users of this keyboard. Important: The following suggestions have not been checked, so if you experience any difficulty, contact us so that we can sort it out and correct any errors on this document, to help others who follow.

Options on the Carter Keyboard. The following options appear to be available and each is listed with a brief comment on the relevance to 'DCR-6' users.

1. Dc-Dc convertor — the -12V supply can be obtained from the ISBUS if you use it, but if not you can fit a convertor, entirely at your option.
2. Alpha Lock Circuit — This is not needed at this stage (non of our software accepts lower case alpha characters)
3. 1ms strobe pulse — A pulsed strobe is not needed, the DCR-6 has a 4528 monostable which generates the required pulse from either a pulse input or a level change.
4. Data strobe invert — If the DCR-6 has an 81LS96 buffer it expects inverted data, (to suit most keyboards), therefore the D.S.I line on the Carter keyboard should be tied to +5V.
5. Parity Invert — The Carter keyboard can be set to give odd or even parity, it doesn't matter which as the software does not read it.

(Note: if you do require a 5V to -12V converter we can supply a type ADIN-12A10 for £4.95 + VAT etc., but we are uncertain whether this will suit the Carter Keyboard).

Carter Keyboard Connector Pins used

Carter Keyboard Signal Name		DCR-6 Board Signal Name	
B1		KDØ	7 BIT ASCII DATA (NEGATIVE TRUE IF 81LS96 IS USED FOR ICS)
B2		KD1	
B3		KD2	
B4		KD3	
B5		KD4	
B6A or B6B (Use B6A or B6B see Note below)		KD5	
B7		KD6	
+STROBE (LEVEL)		S	KEYBOARD STROBE

Note on 'B6A or B6B' If B6A (UC/LC) is connected to KD5 a different code will be sent (and received) according to whether an 'upper case' (e.g A, B, C, D) or 'lower case' (e.g a, b, c, d) letter is selected on the keyboard. As our software does not recognise 'lower case' letters we suggest the alternative B6B (UC) output from the keyboard instead (connected to KD5). In this case the keyboard will substitute the 'upper case' ASCII code whenever a 'lower case' alphabetic chararacter is selected on the keyboard.

DCR-6 Links L1, L2.

The links L1 and L2 adust the polarity and timing of the strobe pulse presented to the data bus when a key is pressed to select a character on the keyboard.

Taking the candidates, 'Miss World' fashion, i.e. in reverse order:- The system data bus requires a short positive, (_⊓_), pulse on the most significant line ('D7', or 'DB7' in ISBUS systems). As IC5 is an inverting buffer if the 81LS96 option has been installed in this position, then the corresponding input, pin 2, has to be an inverted version of the required output (i.e. '⊓' is the shape of the input).

This needs to be taken from the '$\bar{Q}$' output of IC15 (4528), i.e. pin 9, and L1 should therefore be in the short position.

The 'strobe (level)' output from the Carter Keyboard goes high and stays high when the data lines are valid, after a character is selected on the keyboard. The 4528 monostable, IC15 on the DCR-6 board, needs to be triggered when data is valid; in this case on the positive (_⌐) edge of the keyboard strobe. This means that the keyboard strobe should be connected to the '+TR' input of the IC5 4528, i.e. pin 12, and L2 should therefore be connected in the long position.

Use of DCR-6 in Z80 systems (e.g. MZB-3 as CPU).

The DCR-6 is ideally suited for providing some of the 'awkward' functions for the SC/MP microprocessor - e.g. address latch, and page selects for very old systems which do not have a 16-bit address bus. A page select signal is used for the VDU-G card of the VDU-A,B,G set because, due to shortage of edge connector pins it is one card which only has a 12-bit address bus.

Ironically, even the Z80 needs an address latch on the top four bits, so that it can cater for dynamic RAMs, but this has been included on the MZB-3 board, and does not need duplicating here. The MPA-7 SC/MP CPU board also has its latch on the CPU board itself and again it is therefore not needed here as well.

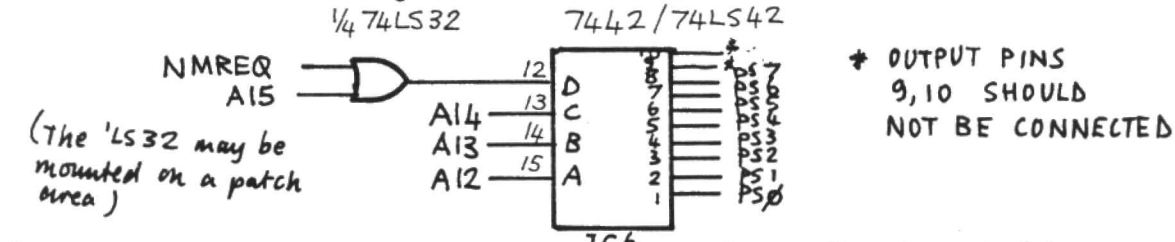
In such systems IC3 and IC4 on the DCR-6 board can simply be removed. (The latch IC4 could alternatively be left in and 'clocked' by some other signal - a typical use would be to turn a small relay or loudspeaker on under computer control for some special purpose).

No more will be said regarding SC/MP systems and the DCR-6, as the point of these notes is to aid the Z80 user. The Z80 issues two sets of addresses on the same address bus: 64K of memory (with NMREQ active), and 256 bytes of 'I/O' (with NI/OREQ active). Early software expects that the VDU and keyboard will be part of the memory space and so the DCR-6 board will need to be modified to respond only when NMREQ is present. A similar, but different, modification is needed if the keyboard is in the I/O space, ie the keyboard part of the DCR-6 must then respond only when NI/O REQ is present. It is likely that in the future the keyboard will be thought of as I/O rather than memory.

A note is available from us which describes the possible changes which may be made to the addressing arrangements in the future. (Ask for 'AN-C23', we may make a small charge later, but it is free at the moment).

In its standard form the devices addressed by the DCR-6 will respond to both a memory address and an I/O address, possibly preventing or limiting the use of I/O ports.

One method to bring in NMREQ is as follows



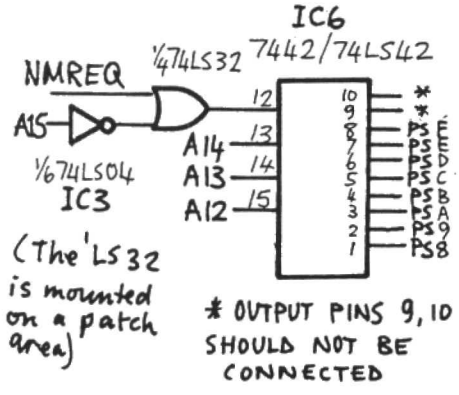
The outputs will then be as shown in the following table

NMREQ	A15	A14	A13	A12	PAGE SELECTED (ALL OTHERS HIGH)
Ø	Ø	Ø	Ø	Ø	PSØ
Ø	Ø	Ø	Ø	1	PS1
Ø	Ø	Ø	1	Ø	PS2
Ø	Ø	Ø	1	1	PS3
Ø	Ø	1	Ø	Ø	PS4
Ø	Ø	1	Ø	1	PS5
Ø	Ø	1	1	Ø	PS6
Ø	Ø	1	1	1	PS7
Ø	1	Ø	Ø	Ø	NONE SELECTED, PSØ - PS7 ALL HIGH
Ø	1	Ø	Ø	1	"
Ø	1	Ø	1	Ø	"
Ø	1	Ø	1	1	"
Ø	1	1	Ø	Ø	"
Ø	1	1	Ø	1	"
Ø	1	1	1	Ø	"
Ø	1	1	1	1	"
1	X	X	X	X	"

'X' = 'DON'T CARE'

If the CPU issues an I/O address, then NMREQ will be high, and as shown in the bottom line of the table, NMREQ being high causes no pages to be selected whatever the state of the address lines.

If the application requires pages above Page 9 then these can be obtained by inverting the A15 line (e.g using part of IC3 74LS04) the circuit and table of outputs is given below.



NMREQ	A15	A14	A13	A12	PAGE SELECTED (ALL OTHERS HIGH)
Ø	Ø	Ø	Ø	Ø	NONE SELECTED
Ø	Ø	Ø	Ø	1	"
Ø	Ø	Ø	1	Ø	"
Ø	Ø	Ø	1	1	"
Ø	Ø	1	Ø	Ø	"
Ø	Ø	1	Ø	1	"
Ø	Ø	1	1	Ø	"
Ø	Ø	1	1	1	"
Ø	1	Ø	Ø	Ø	PS8 (WAS PSØ)
Ø	1	Ø	Ø	1	9 (WAS PS1)
Ø	1	Ø	1	Ø	A (WAS PS2)
Ø	1	Ø	1	1	B (WAS PS3)
Ø	1	1	Ø	Ø	C (WAS PS4)
Ø	1	1	Ø	1	D (WAS PS5)
Ø	1	1	1	Ø	E (WAS PS6)
Ø	1	1	1	1	F (WAS PS7)
1	X	X	X	X	NONE SELECTED, ALL HIGH

'X' = 'DON'T CARE'

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